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High-pressure discharge lamp and method of manufacturing an electrode feedthrough for such a lamp

The invention relates to a high-pressure discharge lamp provided with a discharge vessel having a wall of a ceramic material, and provided with at least one electrode feedthrough comprising a cermet rod, which is secured, at a first end, to a first end of an electrode pin by means of a welded joint, which electrode pin is substantially composed of tungsten and extends in line with the cermet rod. The invention further relates to a method of manufacturing an electrode feedthrough for such a high-pressure discharge lamp.

A lamp of the type described in the opening paragraph is known from European patent application EP 0 887 839 A2. Said known lamp is a high-pressure discharge lamp, more particularly a metal-halide lamp. This lamp has a discharge vessel of a ceramic material and is provided with two electrode feedthroughs comprising a cermet rod. In this description and in the claims, ceramic material is to be taken to mean a densely sintered polycrystalline metal oxide, such as aluminum oxide or yttrium aluminum garnet, or a densely sintered polycrystalline metal nitride, such as aluminum nitride. In this description and in the claims, cermet is to be taken to mean a sintered compound of a mixture of ceramic material and a metal, in particular a mixture of aluminum oxide and molybdenum. Such cermets are refractory materials having electroconductive properties. Particularly the cermets of aluminum oxide, which comprise 35 to 70% molybdenum, are found to be very suitable for use in the electrode

feedthrough of high-pressure discharge lamps. The cermet rod of the electrode feedthrough of the known lamp is secured to an electrode pin by means of a welded joint, said electrode pin being predominantly composed of tungsten. Said joint between cermet rod and electrode pin is embodied so as to be a butt weld, with an end of the cermet rod being pressed against an end of the electrode pin by exerting a small force, and the weld being formed by directing a laser beam at the interface between the rod and the pin.

The electrode feedthrough of the known lamp has a number of drawbacks. As a result of the operation wherein laser beams are used to produce the welded joint between the cermet rod and the electrode pin, comparatively large quantities of impurities are obtained on the electrode feedthrough and on the tools. These impurities consist in particular of aluminum oxide originating from the cermet rod as a result of evaporation at the location where the laser beam is incident on the rod. This problem is aggravated when use is made of cermet rods having a larger diameter and cermet materials having a comparatively small molybdenum content. As a result, lamps with a higher wattage and higher current intensities are problematic in practice. In addition, at the location of the welded joint, welding edges are formed which seriously hamper the formation of the electrode feedthrough in the wall of the discharge vessel.

It is an object of the invention to provide measures by means of which said drawbacks can be obviated.

A high-pressure discharge lamp of the type mentioned in the opening paragraph is characterized in accordance with the invention in that the electrode pin comprises a solidified tungsten melt at its first end in the vicinity of the interface between electrode pin and cermet rod.

It has been found that a good welded joint between cermet rod and electrode pin can be obtained if, in the course of the welding process, the welding energy is supplied to the electrode pin in an area near the interface between rod and pin, which area does not extend up to the cermet rod, so that direct heating of the cermet is precluded. This area is hereinafter referred to as the welding area. A prerequisite is that

the welding area is situated near the interface, i.e. the distance from the center or middle point of the welding area to said interface is at the most equal to half the diameter of the pin. In addition, the welding energy level should be so high that a solidified tungsten melt is formed on the electrode pin at the location of the welding area. At this choice of the welding area and at such values of the welding energy, the first end of the electrode pin is heated to such a high temperature that the temperature of the cermet rod at its first end rises above the melting points of the constituent components of the cermet, so that a welded joint is formed at the interface between rod and pin.

An advantage of a lamp in accordance with the invention resides in that the electrode feedthrough exhibits (substantially) no impurities because evaporation of cermet is precluded. This also has advantages for the manufacture of the feedthroughs because soiling of the tools is precluded. In addition, it is advantageous that a lamp in accordance with the invention does not comprise disturbing welding edges or welding drips at the interface between cermet rod and electrode pin.

Lamps in accordance with the invention are preferred wherein the solidified tungsten melt has a dimension that is at most equal to the diameter of the electrode pin, and the distance from said solidified tungsten to the interface between electrode pin and cermet rod is smaller than half the diameter of the electrode pin. In such lamps, the size of the area to which the welding energy is supplied is at most equal to the diameter of the electrode pin, and the welding area is situated very close to the interface between pin and rod, so that a minimum amount of the welding energy is lost in the process wherein the welded joint is formed. The solidified tungsten, however, should not extend beyond the interface.

In a further preferred embodiment of a lamp in accordance with the invention, the electrode pin exhibits, at its first end, a tungsten melt in three locations on its circumference, which tungsten melts are arranged at an angle of 120° with respect to each other and are at the same distance from the interface. This embodiment enables a very reliable welded joint between cermet rod and electrode pin to be achieved, because during forming the welded joint, the welding energy is supplied, for example by means of

three laser beams, in a substantially homogeneously distributed manner to the first end of the electrode pin in a location very close to the interface between rod and pin.

In a practical embodiment of a lamp in accordance with the invention, the cermet rod of the electrode feedthrough is connected by its second end to a niobium pin. The reason for this being that a reliable current supply to the lamp is thus obtained.

Preferably, a lamp in accordance with the invention comprises an electrode pin carrying, at its second end, a tungsten electrode spiral. By virtue thereof, the emission properties of the electrode pin are improved.

A method of manufacturing an electrode feedthrough of a high-pressure discharge lamp in accordance with the invention is characterized in that a cermet rod is arranged such that a first end butts against a first end of a substantially tungsten electrode pin situated in line with the cermet rod, and in that a laser beam is directed at the first end of the electrode pin, at a target point in the vicinity of the interface between electrode pin and cermet rod, as a result of which a welded joint is obtained at the interface between cermet rod and electrode pin and, in addition, a melt, which solidifies upon cooling, is formed at the target point on the first end of the electrode pin.

A method in accordance with the invention has the advantage that the welding energy can be very accurately supplied to the desired location near the interface between cermet rod and electrode pin, as a result of which, on the one hand, impurities are precluded and, on the other hand, welding edges and fins at the cermet rod are avoided.

Preferably use is made of a method in accordance with the invention wherein two or more laser beams are directed at two or more target points on the circumference of the first end of the electrode pin, which target points are situated on the circumference of the electrode pin so as to make equal angles with each other and are situated at an equal distance from the interface between electrode pin and cermet rod. It has been found that this method enables reliable welded joints to be obtained, which can be reproduced very readily. After all, the welding process is only slightly influenced by small variations in the applied welding energy, the diameter of the target points and the focusing of the laser beams. In addition, the welding process is substantially independent

of the diameter and the composition of the cermet rod. The method proves to be particularly suitable for electrode pins having larger diameters, for example 1.0 mm or more. It has been found that, in this method, the use of three laser beams arranged so as to make an angle of 120° with each other leads, in practice, to very good results. In addition, the welding energy is reproducibly supplied in a well-localized manner to the desired locations near the interface.

These and other aspects of the lamp and the method in accordance with the invention are apparent from and will be elucidated with reference to a drawing, wherein

Fig. 1 diagrammatically shows a side view, partly in section, of a lamp in accordance with the invention; and

Fig. 2 shows the electrode feedthrough of the lamp in accordance with Fig. 1 in more detail.

Fig. 1 shows a high-pressure discharge lamp with a discharge vessel 1, which is provided with an ionizable filling containing metal halide. The lamp has a power of 400 W. The discharge vessel 1 is made from densely sintered polycrystalline aluminum oxide, and provided with two electrode feedthroughs 2 and 3. By means of a sealing glass the feedthrough 2 is connected in a vacuumtight manner to a densely sintered aluminum oxide tube 4 which is sintered into the end wall 5 of the discharge vessel 1. The electrode feedthrough 2 comprises a cermet rod 6 which is secured, at its first end 7, to the first end 8 of an electrode pin 9 by means of a welded joint. The cermet rod is composed of a sintered mixture of aluminum oxide and 35% molybdenum. The material of the electrode pin is tungsten, which may be doped with, for example, K and/or Re, or a tungsten alloy doped with, for example, Re. The cermet rod 6 is connected by its second end 12 to a niobium pin 13, and the electrode pin 9 carries a tungsten electrode spiral 11 at its second end 10.

Fig. 2 is a more detailed view of the electrode feedthrough of the lamp shown in Fig. 1. The cermet rod 26 has a diameter of 2.05 mm and is secured, at its first end 27, to the first end 28 of the tungsten pin 29 by means of a welded joint. The pin 29 has a diameter of 1.18 mm and carries the electrode spiral 31 at its second end 30. Near the interface 34 between the pin and the rod, the pin exhibits a solidified tungsten melt 35, which is caused by applying the welding energy to said location during the manufacture of the electrode feedthrough. The melt 35 has a diameter of 0.6 mm and extends to approximately 0.1 mm from the interface 34. The melt 35 does not contact the interface 34. In addition, damages such as welding edges and fins on the cermet rod do not occur. The distance between the melt 35 and the interface 34 (the distance from the middle point of the melt to the interface) is approximately 0.4 mm. This distance should generally not exceed the diameter of the tungsten pin in order to allow the temperature of the first end of the cermet rod to be sufficiently high, during the manufacture of the electrode feedthrough, to form a welded joint at the interface 34. At its first end 28, the tungsten pin 29 has a second solidified tungsten melt (not shown in the drawing) of substantially the same dimensions as the melt 35, which second solidified tungsten melt is situated diametrically opposite the solidified melt 35 and at the same distance from the interface 34. After all, during manufacturing the welded joint, the welding energy is substantially equally distributed to the relevant places on the electrode pin.

Electrode feedthroughs of the type described above were manufactured as follows. A cermet rod having a diameter of 2.05 mm was pressed against a tungsten electrode pin having a diameter of 1.18 mm by applying a force of 1 to 2 N, which rod and pin remained freely movable in the axial direction. Subsequently, a laser whose power was set to 4 kW was used to generate a laser pulse with a pulse duration of 20 ms, the laser beam being divided into two sub-beams, which sub-beams were focused on diametrically opposite target points on the first end of the tungsten pin near the interface between rod and pin. The diameter of the sub-beams on the target spots was 0.6 mm, and the distance from the middle point of the target points to the interface was 0.4 mm. The energy supplied by the laser pulse was 80 J. In this manner, a strong welded joint was obtained between cermet rod and electrode pin, with a tungsten melt, that solidified upon

cooling, being formed at the target points of the laser beams. This method was found to be readily reproducible and only little dependent on small variations in process parameters.

~~Electric device with data communication bus~~

~~The invention relates to an electronic device, comprising:~~

~~a data communication bus having a plurality of substantially parallel conductors, the plurality of substantially parallel conductors comprising a first conductor and a second conductor; and~~

~~a control circuit for providing the first conductor with a first electrical signal and the second conductor with a second electrical signal.~~

~~In the art of integrated circuit (IC) design, data communication buses, e.g. communication devices for connecting at least one sender to at least one receiver, are well-known devices for establishing high-speed communication between various components e.g. processors, cores, memories, peripherals and so on. With the ongoing downscaling of the dimensions of semiconductor devices, the distances between the conductors of the data communication buses become smaller, which introduces various interference problems. This can be explained in terms of a mutual capacitance (Cm) of neighboring conductors, which becomes larger with the aforementioned decrease in technology dimensions. It is expected that Cm will become so large that it will dominate the transient behavior of the conductors. Two major unwanted effects arise from this. First of all, additional noise, e.g. crosstalk, is introduced with increasing Cm, leading to a deterioration of signal integrity and increase of communication latencies because more time is required to charge Cm. Moreover, power consumption increases as a result of the~~

~~larger Cm. For instance, for a 0→1 transition next to a 1→0 transition on two adjacent conductors the polarity of the voltage on the capacitor is reversed; first the capacitor has to be discharged before it can be charged again which increases both power consumption and signal propagation delay when Cm becomes larger. Since the power consumption increases with the downscaling of semiconductor device dimensions, the increase in power consumption associated with an increasing Cm is a highly unwanted effect, because these power issues are increasingly becoming a limiting factor to integration density.~~

~~In the proceedings of the DATE conference 2000, "A Bus Delay Reduction Technique Considering Crosstalk" on p. 446 by K. Hiroshe and H. Yasuura, a data communication bus with inverter chains of different lengths coupled to the various conductors has been disclosed. This results in a reduction of crosstalk associated with opposite transitions, because the temporal overlap between the rising and falling edge of the respective transistions is reduced. In other words, a (01) → (10) transition, with the bracketed values representing the signal values on two neighboring conductors, proceeds via a (11) or (00) intermediate state, depending on which transition exhibits the longer delay.~~

~~It is a disadvantage of the aforementioned arrangement that the symmetrical e.g. (00) →(11) and (11) →(00) transitions are also selectively delayed. In both the (00) and (11) states, the mutual capacitor Cm is uncharged, and as long as the (00) →(11) and (11) →(00) transitions take place simultaneously no charging of Cm is required. If, however, a delay is introduced in one of the transitions with respect to the other, the (00) →(11) transition proceeds via a (01) or (10) state with associated charging and discharging of Cm. Although the aforementioned arrangement improves overall signal integrity, it is a disadvantage that the power consumption of the bus communication is increased for certain transitions.~~

~~Inter alia, it is an object of the present invention to provide a data communication bus of the kind described in the opening paragraph for which the overall power consumption associated with signal transitions on the conductors of a data communication bus is reduced.~~

~~Now, this object is realized by first signal transition dependent delay circuit for delaying a first electrical signal transition; and second signal transition dependent delay circuit for delaying a second electrical signal transition.~~
~~The delay of a 0 → 1 or a 1 → 0 transition causes the (01) → (10) and (10) → (01) transitions to take place through an intermediate (11) or (00) state, thus yielding a reduction in power consumption, because a full reversal of the capacitor polarity associated with the direct (01) → (10) and (10) → (01) transitions is avoided by the intermediate (11) or (00) states, in which the capacitor is uncharged. Preferably, the first and second delay circuits introduce a substantially equal delay. As a consequence, each of the (00) → (11) and (11) → (00) transitions is then delayed by substantially the same amount of time, which prevents the occurrence of the unwanted intermediate (10) and (01) states during symmetrical transitions, thus avoiding the unneccesary charging of Cm. Consequently, a significant power reduction is achieved.~~

~~It is an advantage if the first signal transition dependent delay circuit comprises a logic element having a first input being coupled to an input of the delay circuit via a first input delay element; a second input being coupled to the input of the delay circuit; and an output being coupled to the first conductor.~~
~~Logic elements are very suitable elements for introducing a transition dependent delay, because only specific transitions cause a change in the output value of a logic element. In addition, the transition characteristics of standard logic elements usually are designed to be highly symmetrical, i.e. the rising edges and falling edges of the respective 0 → 1 and 1 → 0 transitions are very similarly shaped, which is advantageous in terms of signal integrity.~~

~~It is an advantage if the logic element comprises an AND gate, and the first input delay element comprises an inverter chain having an even number of inverters. Driving a signal through both inputs of an AND gate, whereby one of the inputs is delayed with respect to the other input, the 0 → 1 transition on a conductor is delayed, whereas the 1 → 0 transition is not, because for the 0 → 1 transition both inputs of the AND gate have to reach the '1' state as opposed to the 1 → 0 transition, where the less delayed input reaching a'0' state wil already cause the AND gate to output a logic 0.~~

~~It is another advantage if the logic element comprises a NOR gate; the first input delay element comprises an inverter chain having an even number of inverters and the first input and second input of the logic element being coupled to the input of the first transition dependent delay circuit via an inverter. Driving a signal through both inputs of a NOR gate, whereby one of the inputs is delayed with respect to the other input path, the 0 → 1 transition on a conductor is delayed, whereas the 1 → 0 transition is not, because for the 0 → 1 transition both inputs of the NOR gate have to reach the '0' state as opposed to the 1 → 0 transition, where the less delayed input reaching a'1' state wil already cause the NOR gate to output a logic 0.~~

~~It is noted that in US patent 4,905,192 a semiconductor memory is disclosed. In this patent, the aforementioned delay elements, e.g. the NOR and AND gate, can be found in Fig.7 and 8 respectively. However, in this patent the transition dependent delay circuits are exclusively being used in memory devices to generate a word line driver signal only after a decoder inhibit signal is generated, in order to provide high speed access to a memory when the redundancy circuit is not used, as stipulated in col. 1 lines 16-63, col. 2 lines 14-15 and col. 5 lines 6-16. As clearly stated in col. 1 lines 56-63, the motivation for using transition dependent delay circuit is to set optimum timings in both cases where the redundancy circuit is used and not used. It is emphasized that the aforementioned prior art is silent about the effect of introducing transition dependent delays to reduce power consumption in high-speed communication devices e.g. data communication buses. In addition, the use of transition dependent delays in bus communications introduces asymmetry in the timing of the rising and falling edges of the~~

~~signal on the bus conductors, which is a contra-intuitive concept in a technical field where signal symmetry is considered to be an advantageous characteristic. Consequently, it is stipulated that the use of transition dependent delay circuit to reduce power consumption is a novel and non-obvious application of the transition dependent delay circuit.~~

~~It is a further advantage if the first signal transition dependent delay circuit comprises an asymmetric inverter having an input coupled to the control circuit; an output coupled to the first conductor; a first transistor having a first resistance; and a second transistor having a second resistance.~~

~~The use of an inverter having transistors with different resistances also introduces transition dependent delays. In conventional inverters, the width over length (W/L) ratio of the transistors is chosen such that both transistors exhibit comparable resistances to ensure symmetrical rising and falling edges in the switching behavior. As a result of the adjustment of the W/L ratio of at least one of the transistors, the transistor with the smaller ratio will take longer to become conductive due to its increased resistance and as a result the transition of the signal associated with the conductivity of that transistor will become delayed.~~

~~For the previous embodiment, it is another advantage if the output of the asymmetric inverter is coupled to the first conductor via a capacitor and a buffer circuit. To compensate for the introduced asymmetries between the shape of the rising and falling edges of the signal, the asymmetric inverter is coupled to a capacitor and a buffer circuit, which will create similar edge shapes once the respective transistors become conductive.~~

~~The invention is described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:~~

~~Fig.1 shows the electronic device according to the present invention,~~

~~Fig. 2 shows a schematic layout of a number of data bus conductors and accompanying capacitances,~~

~~Fig.3 shows a transition dependent delay circuit of the electronic device according to an embodiment of the present invention,~~

~~Fig.4 shows a transition dependent delay circuit of the electronic device according to another embodiment of the present invention, and~~

~~Fig. 5 shows a transition dependent delay circuit of the electronic device according to yet another embodiment of the present invention.~~

~~In Fig.1, an electronic device 10 has a data communication bus 12. The electronic device 10 can be a microprocessor, an integrated circuit, a multiple chip module or any other semiconductor device utilizing a data communication bus 12 to enable communication between the various components of the electronic device 10, e.g. memory, CPU, data storage means, peripheral devices and so on. Data communication bus 12 embodies a plurality of substantially parallel conductors 12a, 12b, 12c, 12d with a first conductor 12a and a second conductor 12b, the exact number of conductors being governed by the required bandwidth of the data communication having to take place on the bus 12. Control circuit 14 drives an electrical signal onto the conductors 12a-d. Now, according to the invention, this arrangement is extended with a first transition dependent delay circuit 16a coupling control circuit 14 to first conductor 12a and second transition dependent delay circuit 16b coupling control circuit 14 to second conductor 12b. For reasons of clarity, an input 31 of delay circuit 16a is explicitly shown. It is emphasized that the inclusion of input 31 does not necessarily suggest the requirement of additional hardware for first delay circuit 16a, nor does it suggest a necessary difference between first delay circuit 16a and the other delay circuits 16b-d. Preferably, this arrangement is extended to all conductors 12a-d present in data communication bus 12; i.e. transition dependent delay circuits 16c and 16d are coupled between control circuit 14 and conductors 12c and 12d respectively. In addition, it is preferable that delay circuits 16a-d introduce substantially equal delays for reasons that will be discussed in more detail later.~~

~~It is emphasized that this arrangement is shown as a mere example; it will be obvious to anyone skilled in the art that this arrangement can easily be extended~~

~~and/or altered without departing from the scope of the invention. In addition, although transition dependent delay circuits 16a-d are shown outside control circuit 14, it will be obvious to those skilled in the art that delay circuits 16a-d can alternatively be integrated in control circuit 14.~~

~~The following Figs will be described with backreference to the detailed description of Fig.1, and reference numerals introduced in Fig.1 will have the same meaning unless stated otherwise.~~

~~The power reduction associated with the presence of transition dependent delay circuits 16a-d will be explained in more detail with the aid of Fig.2. In CMOS technology, the behavior of conductors 12a-d is dominated by two capacitances: the mutual capacitance Cm between two neighboring conductors e.g. conductor 12a and conductor 12b and so on, and the base capacitance Cb, which is the capacitance between conductor 12a and the substrate 22. Obviously, the latter also holds for conductors 12b-d. With the downscaling of CMOS technology, the distance between neighboring conductors 12a-d in a data communication bus 12 decreases, which increases Cm. Cb is less sensitive to the downscaling, and, consequently, Cm will dominate the switching behavior of data communication bus 12 with the ongoing downscaling into the deep submicron domain. This has a detrimental effect on the power consumption of data communication bus 12, as will be demonstrated below. As a simple example, in Table I the charge that has to be stored in Cm by power supply (ΔQ_{supp}) associated with an undelayed and delayed simultaneous signal transition on two neighboring wires is given.~~

~~Table I~~

	~~transition (12a 12b)~~	~~additional delay*~~	~~Cm polarity~~	~~ΔQ_{supp}~~
~~(a)~~	~~(00) → (11)~~	~~none~~	~~0 → 0~~	~~0~~
~~(b)~~	~~(00) → (01) → (11)~~	~~0 → 1 (12a)~~	~~0 → (-/+) → 0~~	~~$-C_m$.V~~
~~(c)~~	~~(10) → (01)~~	~~none~~	~~(+/-) → (-/+)~~	~~$-C_m$.2V~~
~~(d)~~	~~(10) → (11) → (01)~~	~~1 → 0 (12a)~~	~~(+/-) → 0 → (-/+)~~	~~$-C_m$.V~~

~~* on one of the two conductors~~

~~In entry (a), the effect of an undelayed, or equally delayed, (00) → (11) signal transition on neigbouring conductors 12a and 12b is given. In the initial (00) state capacitor Cm is uncharged and because no voltage difference occurs between conductors 12a and 12b during the transition, capacitor Cm remains uncharged all through the transition; hence the charge transferred from power supply to Cm remains zero.~~

~~In entry (b), the effects of a delay on the (00) → (11) signal transition of one of the neighboring conductors 12a and 12b are given. Here, the 0 →1 transition on conductor 12a is delayed, leading to an intermediate voltage difference between conductor 12a and conductor 12b at intermediate state (01). In the intermediate state, capacitor Cm becomes charged with a polarity (-/+), in which the left sign denoted the polarity of the capacitor plate on the side of conductor 12a and the right sign denotes the polarity of the plate on the side of conductor 12b. Consequently, capacitor Cm with capacitance C_m will approximately be charged corresponding to C_m.V, with V being the voltage difference.~~

~~In entry (c), the effects of an undelayed, or mutually delayed, (10) → (01) signal transition on neigbouring conductors 12a and 12b are given. Here, the polarity of the plates of capacitor Cm both has to be reversed from initial state (+/-) to final state (-/+). This is associated with a charge of approximately C_m.2V having to be provided by the power supply. It is emphasized that this particular transition induces the largest charge flux from power supply to Cm, and is therefore associated with the highest peak current.~~

~~In entry (d), the effects of an delayed (10) → (01) signal transition on neigbouring conductors 12a and 12b are given. Here, the 1 →0 transition on conductor 12a is delayed leading to an intermediate state (11) in the switching process. During this intermediate state, Cm is short-circuited via the power supply and the charge stored on Cm is equalized. Consequently, now Cm only has to be charged from a 0 →(-/+) state,~~

~~which is associated with a charge of approximately C_m.V having to be supplied by the power supply.~~

~~The charging behavior of Cm for the various simultaneous signal transitions on neighboring conductor 12a and 12b clearly shows that for symmetric e.g. (00) → (11) transitions, both transitions should be equally delayed as shown in entry (a) to avoid the occurrence of the intermediate (01) state shown in entry (b) with an associated non-zero charge flow from the power supply to mutual capacitor Cm. On the other hand, for antisymmetric e.g. (01) → (10) transitions, one of the transitions has to be delayed to introduce the intermediate (11) or (00) state shown in entry (d), thus reducing the charge flow from power supply to mutual capacitor Cm from C_m.2V associated with the transition in entry (c) to C_m.V. This makes the electronic device 10 of the present invention particularly advantageous, because it combines the transition behavior of advantageous entry (a) and advantageous entry (d); the symmetric transitions on conductors 12a and 12b are either undelayed or mutually delayed by the respective signal transition dependent delay circuits 16a and 16b, whereas one of the antisymmetric transitions on conductors 12a and 12b is selectively delayed by one of the transition dependent delay circuits 16a and 16b and, consequently, the peak currents associated with the antisymmetric signal transitions are reduced.~~

~~It is emphasized that it will be obvious to anyone skilled in the art that a significant power reduction is also achieved when more than two conductors are involved, and that the mirror images of the transitions shown in Table I yield the same behavior in terms of power consumption.~~

~~In Fig. 3, an embodiment of a transition dependent delay circuit 16a that combines the switching behavior of entries (a) and (d) of Table I is given. Obviously, the same embodiment can also be applied to delay circuits 16b-d. A 2-input AND gate 30 with first input 32 and second input 34 is given. The output 37 of AND gate 30 is connected to conductor 12a. The inputs 32 and 34 of AND gate 30 are coupled to control circuit 14 via input 31. Now, the transition dependent delay is introduced by inverter chain 36 or another delay element known from the art. Inverter chain 36 is inserted into~~

~~the path of first input 32. This has the following effect. For a 1 →0 transition, the logic '0' will be immediately propagated along second input 34, and AND gate 30 will immediately switch to a logic '0'. Therefore, the 1 →0 transition is not delayed by this delay circuit 16a. However, a 0 →1 transition will be delayed, because the 0 →1 transition along first input 32 will be delayed by inverter chain 36. It is emphasized that in this arrangement inverter chain 36 needs to embody an even number of inverters to ensure the correct logic value reaching AND gate 30. AND gate 30 changes the signal value on its output 37 from a logic '0' to a logic '1' not earlier than that the logic '1' has rippled through the inverter chain 36, which effectively delays the 0 →1 transition at conductor 12a. It is emphasized that, although no delay element is shown in the path of second input 34, it does not exclude its presence; the arrangement shown in Fig. 3 merely serves as an example.~~

~~In Fig. 4, another embodiment of transition dependent delay circuit 16a is shown. NOR gate 40 with a first input 42 and a second input 44 and an output 47 coupled to conductor 12a is shown. Again, the same arrangement can also apply to delay circuits 16b-d. Inverter chain 36 is arranged to delay the propagation of the signal coming from control circuit 14 via input 31 along the path of first input 42. In addition, inverter 38 inverts the logic value of the signal coming from control circuit 14 before providing it to first input 42 and second input 44. Again, a 1 →0 transition will not be delayed by inverter chain 36, because as soon as as the logic '0' inverted by inverter 38 into a logic '1' reaches NOR gate 40 through second input 44, NOR gate 40 will output a logic '0' on its output 47 coupled to conductor 12a. For a 0 →1 transition, however, the delay introduced by inverter chain 36 dominates the switching behavior; the logic '0' generated by inverter 38 has to reach NOR gate on both first input 42 and second input 44 before NOR gate 40 switches to a logic '1'. Again, the inverter chain has to embody an even number of inverters to ensure the output of a correct logical value to NOR gate 40.~~

~~It is emphasized AND gate 30 and NOR gate 40 can also be used to delay the 1 →0 transition by applying well-known boolean logic redesign techniques. For example, an inverter not shown can be coupled between the output of AND gate 30 and~~

~~conductor 12a in combination with an inverter not shown coupled to first input 32 and second input 34 similar to the arrangement with inverter 38 shown in Fig. 4. It will be obvious to anyone skilled in the art that many variations to delay circuits 16a-d are possible without departing from the scope of the invention.~~

~~The embodiment of delay circuit 16a shown in Fig. 5 does not incorporate a logic gate to introduce the transition dependent delay. Here, an asymmetric inverter 50 comprising a first transistor 52 and a second transistor 54 is used to introduce a transition dependent delay. The introduction of different dimensions e.g. different W/L ratios for the two transistors invokes asymmetric on/off switching of asymmetric inverter 50. Here, a relatively small pMOS transistor 52 causes a relatively slow 0 →1 transition at the output 57 of asymmetric inverter 50 when the input value provided by control circuit 14 via input 31 becomes low. The relatively slow transition is caused by a relatively high resistance of pMOS transistor 52. On the other hand, a relatively large nMOS transistor 54 causes a relatively fast 1 →0 transition at the output 57 of asymmetric inverter 50 when the input value provided by control circuit 14 becomes high. The relatively fast transition is caused by a relatively low resistance of nMOS transistor 54. Obviously, this behavior can be reversed by interchanging the dimensions of first transistor 52 and second transistor 54. To ensure that the rising and falling edges of the signal outputted to conductor 12a via output 57 are of similar shape, delay circuit 16a is extended with a capacitor 56 and a buffer circuit 58. Buffer circuit 58 preferably comprises an inverter, not shown, to match the logic value outputted to conductor 12a to the logic value inputted from control circuit 14. In this case, the 0 →1 transition outputted to conductor 12a is delayed in comparison to the 1 →0 transition. It is stipulated that other delay circuits e.g. Schmitt trigger gates and comparable circuits can also be used without departing from the scope of the invention.~~

~~It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting~~

~~the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.~~

ABSTRACT:

A high-pressure discharge lamp includes a discharge vessel having a wall of a ceramic material. The lamps also includes at least a feedthrough of an electrode having a cermet rod. The cermet rod is connected at a first end to a first end of a predominantly tungsten electrode pin by a welded joint. The electrode pin is in line with the cermet rod and has, at its first end, a solidified tungsten melt that is located near the interface between electrode pin and cermet rod.